

# Ashwin Rohit Alagiri Rajan

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## EDUCATION

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### University of California, San Diego (UCSD)

*M.S. in Computer Engineering*

La Jolla, CA

Sep. 2024 – Jun. 2026

### University of California, San Diego (UCSD)

*B.S. in Computer Engineering; Warren Provost Honors*

La Jolla, CA

Sep. 2021 – Jun. 2024

## RESEARCH EXPERIENCE

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### Researcher, ACT Lab

*University of California, San Diego*

Jul. 2024 – Present

La Jolla, CA

- Worked under Professor Hadi Esmaeilzadeh at the ACT Lab for robotics accelerator and Secure LLM Inference accelerator projects
- Developed analytic and cycle level simulator for systolic array based robotics workload accelerator for complete End-to-End workload
- Architected visualisation tools and multi-core GPU performance timing utilities for benchmarking Robotics workloads in NVIDIA GPUs and Jetson edge platforms
- Created cycle accurate simulator for Systolic Array based accelerator for Secure LLM Inference workloads
- Created parameterisable visualisation tools for Secure LLM accelerator to identify microarchitectural stall conditions and datapath constraints
- Robotics and Secure LLM Research work under submission in **ISCA 2026**

### Undergraduate Researcher, Kastner Research Group

*University of California, San Diego*

Apr. 2024 – Jan. 2025

La Jolla, CA

- Co-authored and published a peer-reviewed paper at **IGSC/MICRO 2024** by investigating GPU workload performance on repurposed Android devices to reduce the carbon footprint of EdTech
- Pioneered the conversion of the CSE 160 (Parallel Programming) curriculum from CUDA to OpenCL, developing new course assignments to improve cross-platform hardware compatibility
- Served as teaching assistant for CSE 160 with Prof. Ryan Kastner in Winter 2025 and received ~100% positive feedback

### Intern, Qualcomm Institute

*University of California, San Diego*

Jun. 2023 – Jun. 2024

La Jolla, CA

- Developed system for creating a simulation pipeline to recreate personalized Head-Related Transfer Functions (HRTFs) from 3D scanned models
- Initiated move from CUDA to Apple Metal for audio raytracing system to better reach Audio Engineering community

## PROJECTS

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### 2D Systolic Array accelerator for ML workloads | *Verilog, Python, PyTorch*

- Architected 2bit/4bit reconfigurable systolic array with reconfigurable weight and output stationary setup
- Trained and implemented 2bit and 4bit quantised QAT trained VGG-16 and BERT models

### Autonomous UAV | *C++, Python, PX4, Jetson Nano, OpenCV, SLAM*

- Architected and deployed an autonomous UAV on a Jetson Nano (embedded SoC), implementing custom SLAM algorithms for real-time environmental mapping and localization
- Integrated computer vision-based obstacle detection and avoidance using OpenCV within a C++/Python robotics pipeline, ensuring safe navigation in dynamic environments

## TECHNICAL SKILLS

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**Languages:** C, C++, Python, CUDA, Verilog, SystemVerilog, OpenCL, Rust

**Frameworks & Libraries:** PyTorch, TensorFlow, ROS, Kubernetes, Docker, OpenCV, NumPy, Pandas, UVM

**Developer Tools:** Git, Cycle-level Simulators, Analytic Simulators, NVIDIA Jetson Platforms, FPGAs

**Technical Areas:** Computer Architecture (SoC, CPU/GPU), System-Level Modeling, Hardware Acceleration, RTL Design, Machine Learning (LLMs), Robotics, Parallel Computing, Embedded Systems